

IN THE CLAIMS

Please cancel claims 1-8, 16-17 and 19-20.

Please amend the claims as follows.

1-8 (Cancelled)

1 9. (Currently amended) An integrated circuit comprising:
2 a register file bit comprising:
3 a primary latch having a data input and a data output;
4 a plurality of secondary latches each having a data input and a data output;
5 a feedback path from the data output outputs of the plurality of secondary
6 latches to the data input of the first primary latch, the feedback path including a
7 data selection mechanism for selecting one data output only from among each of
8 the data outputs from the plurality of secondary latches to feed back to the data
9 input of the first primary latch; and

10 a context switch mechanism that causes the data on the data output of the
11 primary latch to be written to a selected one of the plurality of secondary latches,
12 and that causes the data on the data output of the selected one secondary latch to
13 be written to the primary latch.

1 10. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
2 comprises a swap signal coupled to the primary latch.

1 11. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
2 comprises a delay element between the data output of the primary latch and the data
3 inputs of the plurality of secondary latches.